



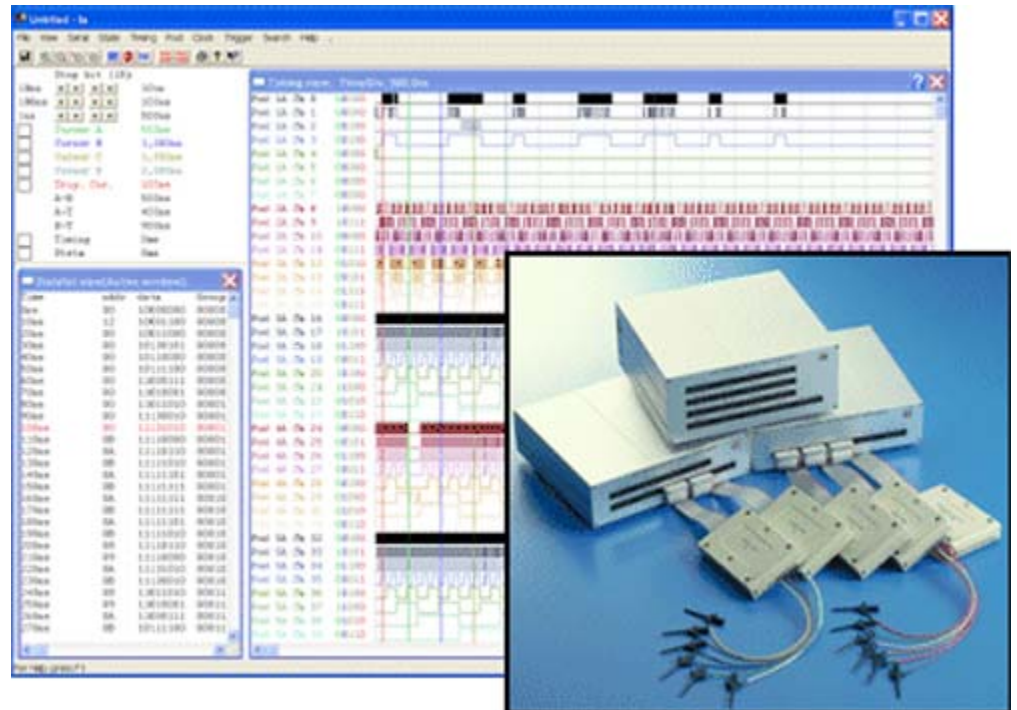
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LA-5000 Series

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[Features](#)
[Specifications](#)
[Screenshots](#)
[Software Updates](#)
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[Pricing](#)
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PRICE

LA-5240
[\\$1700](#)
LA-5280
[\\$2350](#)
LA-5540
[\\$2500](#)
LA-5580
[\\$3500](#)
LA-55160
[\\$7500](#)

The LA-5000 series Logic Analyzers communicate with your PC by USB 2.0 and Parallel port. They offer all of the features and performance you have come to expect: high speed clock rates, deep data buffers, sophisticated triggering, easy data management and large color displays.

The PC-based instruments are controlled with easy to use Windows software. This allows for more organized data display (with color coded data and increased screen size), intuitive user interface, and data management (file saving, loading, sharing and exporting to other software and reports).

Our logic analyzers connect to your PC's parallel port or USB port and take advantage of your large color screen, disk drives and printers. They are compact and don't have screens, drives, knobs or buttons - saving you money and space.

The LA-5000 PC-based logic analyzer series can be configured to be a pattern generator with the purchase of optional [pattern generator pods](#).

The LA-5000 series replaces our LA-4000 series of Logic Analyzers. The new LA's have larger memory and more channels at higher speeds (LA-5540, LA-5580 and LA-55160) and support USB 2.0 and Parallel port communications with the PC.

Features

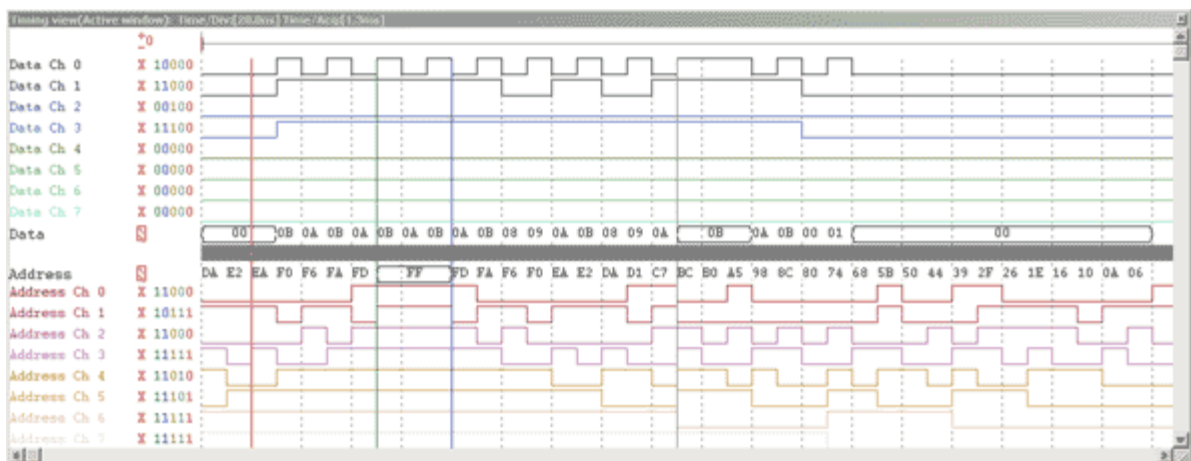
- **Logic Analyzer FrontPanel™ Software**
For Windows XP/2000/NT/ME/95/98
- **40, 80, and 160 Channel Versions**
- **High Speed Operation**
500MHz/200MHz
- **Deep Data Buffers**
Up to 512K samples per channel
- **Advanced Triggering**
16 level sequential triggering, up to 160 bits each
- **Printer Support**
Print data on a Windows compatible printer
- **Data File Save/Export**
Save & export to Excel, Word, Mathcad, etc...
- **I²C Monitor Software (optional)**
Decodes I²C serial bus commands
- **Continuously Variable Pre/Post Trigger Position**
Combined with the large data buffer, provides the power of storing up to 512K events surrounding the trigger point
- **High Impedance Probes**
Minimize interference with test circuit (200KΩ by 3pf)
- **Variable Threshold Voltage**
Threshold range: -6.52V and +6.12V; threshold types including TTL, ECL, 3V logic, CMOS, and RS-232
- **Over Voltage Protection**
- **External Trigger Output**
To trigger other instruments (e.g. scope)
- **Up to 100MHz Data Bandwidth**
- **External Clock Input**
8 high speed clock inputs featuring user definable combinations for flexible clock qualifying
- **Simultaneously Captures Both State & Timing Windows**
- **Pattern Generator Output (optional)**
With rates up to 100 Mpoints/s, from 16 to 160 channels
- **Standard Accessories**
Data pods, clips, wires
- **Flexible Interface Options**
USB or Parallel Port
- **Software Libraries (DLL)**

Logic Analyzer FrontPanel™ Software

The software has the familiar feel of a windows program while giving you a rich set of Logic Analyzer commands. Parameters can be changed on the fly while acquisitions are repeating and the results seen on the updated display. All functions are accessed through pull down menus and dialog boxes. Toolbar icons offer quick access to more frequently used operations.

Timing Window

The data is displayed as a timing waveform. Each channel is displayed with a user-specified color and label. Channels can also be displayed in any sequence and can also be grouped into busses and viewed in ASCII, HEX, decimal, binary, or user defined mnemonics. The display can be zoomed in/out and scrolled to show just a few samples or the entire buffer. This window also has 4 data cursors that can be used to measure time between events or as markers for places of particular interest.



Address 0B 0A 08 09 1F 2B C5

Group of channels displayed in HEX



Group of channels displayed as a waveform

Statelist Window

Statelist view:				
Time	Data	Address	Group 3	Group 4
90ns	00	11100010	01	00001001
100ns	00	11101010	10	00001010
110ns	0B	11110000	11	00001011
120ns	0A	11110110	00	00001100
130ns	0B	11111010	01	00001101
140ns	0A	11111101	10	00001110
150ns	0B	11111111	11	00001111
160ns	0A	11111111	00	00010000
170ns	0B	11111111	01	00010001
180ns	0A	11111101	10	00010010
190ns	0B	11111010	11	00010011
200ns	08	11110110	00	00010100

Data in the Statelist window is organized into groups and displayed in a numeric format (ASCII, binary, HEX, decimal or user defined mnemonics). These groups are user defined and can have from 1 to 32 channels in them. This window has 4 data cursors that can be used to measure time between events or as markers for places of particular interest. These are the same cursors as the ones in the Timing window and can be used as a reference point when viewing data in both windows.

Search Function

Search

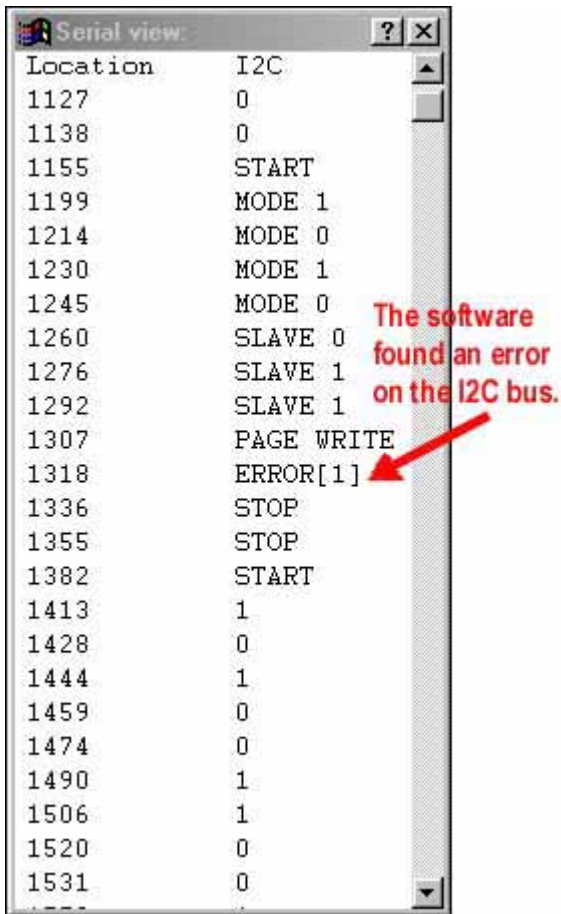
Channels: Ch 0 .. 39

Decimal Pod 5 Pod 4 Pod 3 Pod 2 Pod 1
 Ascii 11111111 11111111 11111111 11111111 11111111
 Hex
 Binary Search backward Search forward OK

Sorting through all your data is easier with our search feature. You can specify a search pattern, including Don't Care bits, in any of the shown numeric bases. Then just click on the forward or backwards search to find what you are looking for.

I²C Monitor Software (optional)

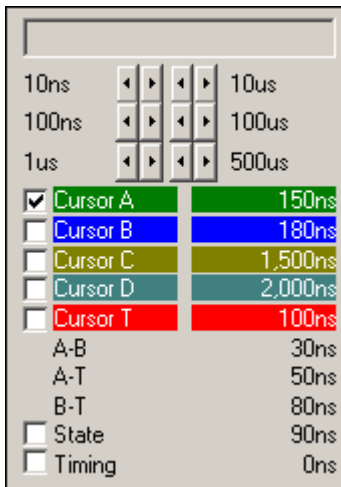
- View I²C codes from a separate window within our Windows based control software.
- Displays I²C commands. Start, Stop, Read, Write, Slave address, Address, Data, ACK and NACK.
- Displays Timing of all activity on the Clock and Data lines showing you everything that happened, including valid I²C codes, glitches, timing errors and other non-I²C data.
- Since this is a logic analyzer, you have plenty of other channels to monitor the rest of your circuit while still viewing the I²C bus.



Location	I2C
1127	0
1138	0
1155	START
1199	MODE 1
1214	MODE 0
1230	MODE 1
1245	MODE 0
1260	SLAVE 0
1276	SLAVE 1
1292	SLAVE 1
1307	PAGE WRITE
1318	ERROR[1]
1336	STOP
1355	STOP
1382	START
1413	1
1428	0
1444	1
1459	0
1474	0
1490	1
1506	1
1520	0
1531	0

- Compare I²C codes with actual circuit behavior. Are your commands actually doing what you expected? You have all of the logic analyzer's resources to verify and debug your circuit response.
- What makes this product so superior to other I²C Monitors is that you are also be able to see all activity on the Clock and Data lines in Timing and Statelist display.

Cursor Controls & Settings



10ns	←	→	←	→	10us
100ns	←	→	←	→	100us
1us	←	→	←	→	500us
<input checked="" type="checkbox"/>	Cursor A				150ns
<input type="checkbox"/>	Cursor B				180ns
<input type="checkbox"/>	Cursor C				1,500ns
<input type="checkbox"/>	Cursor D				2,000ns
<input type="checkbox"/>	Cursor T				100ns
	A-B				30ns
	A-T				50ns
	B-T				80ns
<input type="checkbox"/>	State				90ns
<input type="checkbox"/>	Timing				0ns

The current position of the cursors is shown here. Selecting a specific cursor or display window and then clicking the arrows allow precise changes of position. The cursors can also be quickly repositioned by clicking on the cursor and dragging it.

The position, both absolute and relative to the trigger, can be shown in time units or data sample numbers.

Software Compatibility

OS's supported:	USB 2.0	Parallel Port
Windows XP/2K	✓	✓
Windows NT		✓
Windows 98/98SE/ME	✓	✓
Windows 95		✓

The LA-5000s have software for Win XP, Win 2K, Win NT, Win 95, and Win 98. The logic analyzers are PC-based and we regularly upgrade the software with more features and support for new operating systems. [Software updates](#) are free and available on the website.

Print Support

Statelist and Timing waveforms can be printed on any Windows compatible printer.

File Save/Export

The logic analyzer data can be stored on your PC in a number of ways:

- Files can be saved to disk for future viewing
- Data can be exported in "CSV" format to programs like Mathcad, Excel, Word, etc...
- You can paste screen images into your reports using programs like Word, Excel, image editors, etc...
- Data can even be shared with other computers. You don't need to have our logic analyzer connected to a computer to view the data files. You can capture data in the lab and view it in your office or you can email it to other engineers at remote locations for analysis

High Speed Operation (500MHz/200MHz)

Although theoretically you need your logic analyzer to capture at only twice your data rate, in reality you need much more than that. Our analyzers provide up to 500MHz clock rates for accurate and detailed data capture.



Low speed sample rate (signal appears good)



High speed sample rate (notice the glitch)

Deep Data Buffers (up to 512K samples per channel)

Simply put, the deeper the buffer the better. Our data buffer gives you the flexibility to store a great number of events surrounding the trigger. Sometimes it is difficult to pinpoint the exact event that you want to trigger on. With our system you don't need to know exactly where to trigger since our large buffer will capture so many events. And of course you can capture long events that other analyzers may cut off. Also, you can maintain higher sampling rates to get more detail without running out of buffer space.

Continuously Variable Pre/Post Trigger Position

The continuously variable pre/post trigger positioning enables the user to control the amount of data recorded before and after the trigger event. The trigger cursor can be positioned anywhere in the buffer (up to 512K) so that can see a long train of events that led up to the trigger condition, a long series that followed the trigger or many events surrounding it.

Advanced Triggering

Our logic analyzer captures the data that is important to you. Its sophisticated 16 level triggering (up to 160 bits each) lets you fine tune the exact point to start capturing. Multilevel triggering is used to make the logic analyzer look for a sequence of events to happen (i.e. address xxxx1110xx111x0x followed by address 11xx1110xx111x0x).

Number of Levels	16 sequential trigger levels
Trigger Conditions	0,1 and DON'T CARE for all channels Pass Counter: 1 to 255 Duration Timer: $\leq n$, or $\geq n$ clocks; where n is 1 to 255
Trigger Edge	Trigger on the condition becoming true or becoming false
Trigger Position	Trigger position can be set anywhere in the capture buffer
Trigger Modes	<p>Single: If trigger conditions are met, acquire a buffer worth of data</p> <p>Normal: If trigger conditions are met, acquire a buffer worth of data, then restart</p> <p>Auto: If trigger conditions are not met within a set time, acquire a buffer worth of data, then restart</p>
Trigger Out	BNC connector on rear of logic analyzer

40, 80, and 160 Channel Versions

The logic analyzers have multiple channel/memory/speed modes. Selection is done through the FrontPanel™ software.

LA-5240

Modes (software selectable)	Sampling Rate	Total Channels	Channels/Memory
1	200MSa/s	24 Channels	(16 Ch @200MSa/s, 64KB) & (8 Ch @100MSa/s, 32KB)
2	1Sa/s to 100MSa/s	40 Channels	(40 Ch @1Sa/s to 100MSa/s, 32KB)
3	External	40 Channels	(40 Ch @DC to 50MSa/s, 32KB)

LA-5280

Modes (software selectable)	Sampling Rate	Total Channels	Channels/Memory
1	200MSa/s	48 Channels	(32 Ch @200MSa/s, 64KB) & (16 Ch @100MSa/s, 32KB)
2	1Sa/s to 100MSa/s	80 Channels	(80 Ch @1Sa/s to 100MSa/s, 32KB)
3	External	80 Channels	(80 Ch @DC to 50MSa/s, 32KB)

LA-5540

Modes (software selectable)	Sampling Rate	Total Channels	Channels/Memory
1	500MSa/s	24 Ch	(24 Ch @500MSa/s, 512KB)
2	1Sa/s to 250MSa/s	40 Ch	(40 Ch @1Sa/s to 250MSa/s, 256KB)
3	External	40 Ch	(40 Ch @DC to 80MSa/s, 128KB)

LA-5580

Modes (software selectable)	Sampling Rate	Total Channels	Channels/Memory
1	500MSa/s	32 Ch	(48 Ch @500MSa/s, 512KB)
2	1Sa/s to 100MSa/s	80 Ch	(80 Ch @1Sa/s to 100MSa/s, 128KB)
3	External	80 Ch	(80 Ch @DC to 80MSa/s, 128KB)

LA-55160

Modes (software selectable)	Sampling Rate	Total Channels	Channels/Memory
1	500MSa/s	96 Ch	(96 Ch @500MSa/s, 512KB)
2	1Sa/s to 250MSa/s	160 Ch	(160 Ch @1Sa/s to 250MSa/s, 256KB)
3	External	160 Ch	(160 Ch @DC to 80MSa/s, 128KB)

Over Voltage Protection

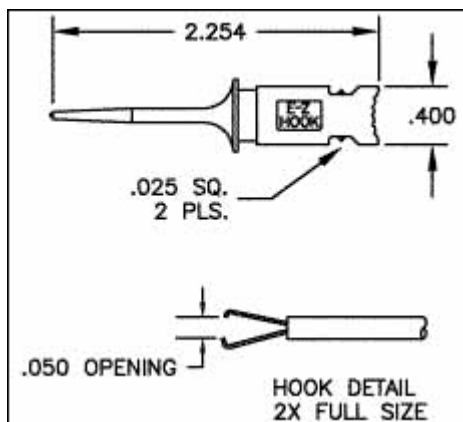
Unlike other analyzers, our LA-5000 series logic analyzers are designed to protect themselves from over voltage damage. If you accidentally touch the wrong pin, you are unlikely to damage anything. The analyzer's logic inputs can handle +/- 120V continuously.

Pattern Generator Output (optional)

With the optional 100 Mpoints/s [pattern generator pods](#) the LA-5000 series logic analyzers can be configured to work as a pattern generator. As few as 16 or as many as 160 channels (max # of channels depends on logic analyzer model) can be configured to output. The remaining channels will continue to function as logic analyzer inputs. The output data can be generated using our software, from your files or acquired through the logic analyzer channels. Output voltage: High: Minimum 2V at 32mA. Low: Maximum 0.55V at 64mA.

Standard Accessories

The standard logic analyzer kit includes software, logic pods, clips and wires.

Clips

The logic analyzer ships with a full set of color coded clips and wires. The double gripper is designed for hard-to-make test connections of varying sizes and shapes. The narrow configuration allows stacking of the test connectors side-by-side for high-density IC packages and surface-mount components. Two 0.025" square pins permit connection to 0.025" square or .030" round push-on adapters or jumpers.

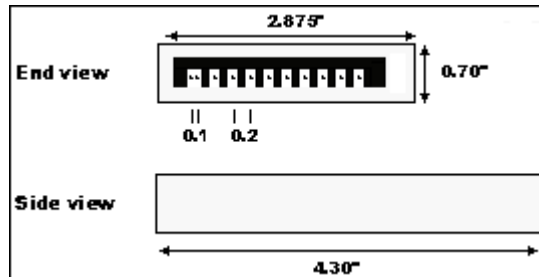
Other options include:

Connecting the wires directly to 0.025" posts on your board and connecting your wires/cables to the posts on the logic pod.

Wires

Wires are used to connect the logic analyzer to either the clips, or directly to the circuit under test. One wire is provided for each channel and two for grounding each data pod. The wires are 10 inches long and have female connectors at each end. These plug onto standard 0.025" posts on your circuit or to the pins on the clips. The other end plugs onto the pins of the data pod.

Data Pods



A complete set of logic analyzer data pods is included. Each pod uses a 13.5" cable (8 data input pins and 3 ground pins) to connect to the analyzer. This is a fully active buffered pod with more than 100MHz digital bandwidth. A full set of clips and wires is included with the logic analyzer. In addition, you can make your own custom wire assembly with a standard header connector.

Flexible Interface Options

The LA-5000 series logic analyzers support both USB 2.0 and parallel port communications with your laptop or desktop Windows computer.

USB 2.0 Support

PICTURE OF USB 2.0 ADAPTER

- Allows connection between an LA-5000 series logic analyzer and the USB 2.0* port of your laptop or desktop computer
- Faster transfer rate
- Compatible with Win XP, Win 2000, Win 99 and Win Me software only

* The adapter will work with USB 1.0 computers also

Parallel Port (printer port) Support

- The LA-5000 directly supports connection to your PC's parallel port.
- Supports EPP, 4 bit and 8 bit parallel communication modes
- Compatible with Win95, Win 98, Win ME, Win NT, Win 2K, and Win XP software only

Specifications

General	
External Clocks	8
Bandwidth	> 100MHz
Setup/Hold Time	2ns/0ns
Threshold Voltage	Variable (-6.52V to +6.12V), each pair of pods can be set to different voltage settings
Impedance	200KΩ shunted by 3pF

Max Input Voltage	Inputs are clamped through a 200K Ω resistor. \pm 150V Cont., 250V Trans.			
Sampling Clock	<p>Model: 5240/5280</p> <p>200MSa, 100MSa, 50MSa, 20MSa, 10MSa, 5MSa, 2MSa, 1MSa, 500Ksa, 200Ksa, 100Ksa, 50Ksa, 20Ksa, 10Ksa, 5Ksa, 2Ksa, 1Ksa, 500Sa, 200Sa, 100Sa, 50Sa, 20Sa, 10Sa, 5Sa, 2Sa and 1Sa</p> <p>Model: 5540/5580/55160</p> <p>500MSa, 250MSa, 100MSa, 50MSa, 20MSa, 10MSa, 5MSa, 2MSa, 1MSa, 500Ksa, 200Ksa, 100Ksa, 50Ksa, 20Ksa, 10Ksa, 5Ksa, 2Ksa, 1Ksa, 500Sa, 200Sa, 100Sa, 50Sa, 20Sa, 10Sa, 5Sa, 2Sa and 1Sa</p>			
External Clock	8 external clocks can be combined to form a versatile sampling clock			
Qualifier	8 external clocks can be used as qualify lines			
Data Skew	Channel to channel, < 2ns typical			
Hardware Compatibility	<p>Parallel Port: EPP, bi-directional, 8bit, 4bit, or normal parallel port</p> <p>USB Port: a USB port is required</p>			
Software Compatibility	<p>Parallel Port: Win XP, Win 2K, Win NT, Win 98, Win ME, Win 95</p> <p>USB Port: Win XP, Win 2K, Win 98, Win ME</p>			
Operating Temperature	50°F to 140°F (10°C to 40°C)			
Configurations				
LA-5240	<p>Modes (software selectable)</p> <p>1</p>	<p>Sampling Rate</p> <p>200MSa/s</p>	<p>Total Channels</p> <p>24 Ch</p>	<p>Channels/Memory</p> <p>(16 Ch @200MSa/s, 64KB) & (8 Ch @100MSa/s, 32KB)</p>
	2	1Sa/s to 100MSa/s	40 Ch	(40 Ch @1Sa/s to 100MSa/s, 32KB)
	3	External	40 Ch	(40 Ch @DC to 50MSa/s, 32KB)
LA-5280	<p>Modes (software selectable)</p> <p>1</p>	<p>Sampling Rate</p> <p>200MSa/s</p>	<p>Total Channels</p> <p>48 Ch</p>	<p>Channels/Memory</p> <p>(32 Ch @200MSa/s, 64KB) & (16 Ch @100MSa/s, 32KB)</p>
	2	1Sa/s to 100MSa/s	80 Ch	(80 Ch @1Sa/s to 100MSa/s, 32KB)
	3	External	80 Ch	(80 Ch @DC to 50MSa/s, 32KB)
LA-5540	<p>Modes (software selectable)</p> <p>1</p>	<p>Sampling Rate</p> <p>500MSa/s</p>	<p>Total Channels</p> <p>24 Ch</p>	<p>Channels/Memory</p> <p>(24 Ch @500MSa/s, 512KB)</p>
	2	1Sa/s to 250MSa/s	40 Ch	(40 Ch @1Sa/s to 250MSa/s, 256KB)
	3	External	40 Ch	(40 Ch @DC to 80MSa/s, 128KB)
LA-5580	<p>Modes (software selectable)</p> <p>1</p>	<p>Sampling Rate</p> <p>500MSa/s</p>	<p>Total Channels</p> <p>32 Ch</p>	<p>Channels/Memory</p> <p>(48 Ch @500MSa/s, 512KB)</p>
	2	1Sa/s to 100MSa/s	80 Ch	(80 Ch @1Sa/s to 100MSa/s, 128KB)
	3	External	80 Ch	(80 Ch @DC to 80MSa/s, 128KB)
LA-55160	<p>Modes (software selectable)</p> <p>1</p>	<p>Sampling Rate</p> <p>500MSa/s</p>	<p>Total Channels</p> <p>96 Ch</p>	<p>Channels/Memory</p> <p>(96 Ch @500MSa/s, 512KB)</p>
	2	1Sa/s to 250MSa/s	160 Ch	(160 Ch @1Sa/s to 250MSa/s, 256KB)
	3	External	160 Ch	(160 Ch @DC to 80MSa/s, 128KB)

Trigger	
Number of Levels	16 sequential trigger levels
Trigger Conditions	0,1 and DON'T CARE for all channels Pass Counter: 1 to 255 Duration Timer: $\leq n$, or $\geq n$ clocks; where n is 1 to 255
Trigger Edge	Trigger on the condition becoming true or becoming false
Trigger Position	Trigger position can be set anywhere in the capture buffer
Trigger Modes	Single: If trigger conditions are met, acquire a buffer worth of data Normal: If trigger conditions are met, acquire a buffer worth of data, then restart Auto: If trigger conditions are not met within a set time, acquire a buffer worth of data, then restart
Trigger In	Any of the logic analyzer inputs can be used as trigger in.
Trigger Out	BNC connector on rear of logic analyzer
Pattern Generator	
Output Voltage	High: Minimum 2V at 32mA Low: Maximum 0.55V at 64mA

Pricing

LA Kit: logic analyzer, data pods, clips, wires, communication adapter (USB or Parallel), International power supply, software

LA-5240	\$1700	
LA-5280	\$2350	
LA-5540	\$2500	
LA-5580	\$3500	
LA-55160	\$7500	
Optional Accessories		
Pattern Generator Pods	\$300 \$250 \$125	<i>1st 16 channels (2 pods, 20 clips, 20 wires), part # LA-PAT-16-1</i> <i>Additional 16 channels (2 pods, 20 clips, 20 wires), part # LA-PAT-16-2</i> <i>Additional 8 channels (1 pod, 10 clips, 10 wires), part # LA-PAT-8</i>
Extra clips and wires	\$165 \$40	<i>50 clips and wires, part # LA-CLIPS-50</i> <i>10 clips and wires, part # LA-CLIPS-10</i>